

Appl. No. 10/708,640
Amdt. dated November 09, 2005
Reply to Office action of August 18, 2005

Amendments to the Claims:

Listing of Claims:

1. (currently amended) A thin-film transistor comprising:

a substrate;

5 a semiconductor layer positioned on the substrate, the semiconductor layer comprising a channel region, two lightly doped drains, and two source/drain regions; and

a gate positioned on the substrate, the two lightly doped drains being symmetrically arranged with respect to the gate, either of the two gate
10 edges being overlapped with the adjacent lightly doped drain, neither of the junctions between the lightly doped drains and the source/drain regions being overlapped with the gate, and neither of the source/drain regions being overlapped with the gate[.];

wherein the gate comprises a length A, the channel region comprises a
15 length B, the lightly doped drains comprise a length C, and a correlation among these lengths is as following: $B+0.2C \leq 0.5A \leq B+0.8C$.

2. (original) The thin-film transistor of claim 1 wherein the gate is positioned above the semiconductor layer.

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3. (original) The thin-film transistor of claim 1 wherein the gate is positioned below the semiconductor layer.

4. (original) The thin-film transistor of claim 1 further comprising an
25 insulating layer positioned between the gate and the semiconductor layer.

5. (original) The thin-film transistor of claim 1 wherein the substrate comprises a glass substrate.

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6. (canceled)

7. (original)The thin-film transistor of claim 1 wherein the lightly doped
5 drains have an equal length.

8. (original)The thin-film transistor of claim 1 wherein a length of the
lightly doped drains is approximately between 0.3-3.5 μ m.

10 9. (original)A thin-film transistor comprising:

a substrate;

a semiconductor layer positioned on the substrate, the semiconductor
layer comprising a channel region, two lightly doped drains, a source and a
drain;

15 an insulating layer positioned on the semiconductor layer; and

a gate positioned on the insulating layer, the gate comprising a gate
edge overlapped with the lightly doped drain adjacent to the drain, the gate
being not overlapped with the junction between the lightly doped drain and
the drain, and the gate being not overlapped with the drain.

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10. (original)The thin-film transistor of claim 9 wherein the gate comprises
another gate edge overlapped with the lightly doped drain adjacent to the
source, but the gate is not overlapped with the junction between the lightly
doped drain and the source, and the gate is not overlapped with the source.

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11. (original)The thin-film transistor of claim 9 wherein the substrate
comprises a glass substrate.

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12. (original)The thin-film transistor of claim 9 wherein the gate comprises a length A, the channel region comprises a length B, the lightly doped drain adjacent to the drain comprise a length C, and a correlation among these lengths is as following: $B+0.2C \leq 0.5A \leq B+0.8C$.

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13. (original)The thin-film transistor of claim 9 wherein the lightly doped drains have an equal length.

14. (original)The thin-film transistor of claim 9 wherein a length of the
10 lightly doped drains is approximately between $0.3-3.5 \mu m$.

15. (original)The thin-film transistor of claim 9 wherein the lightly doped drains are symmetrically arranged with respect to the gate.